August 25, 2015

CMOS Octal Latching Bus Driver

Features

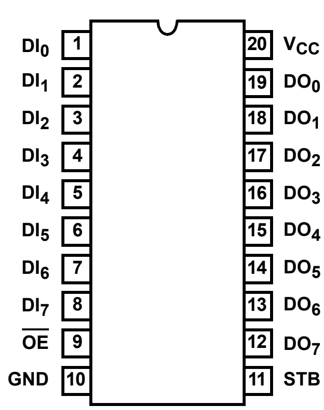
- **Full Eight-Bit Parallel Latching Buffer**
- **Bipolar 8282 Compatible**
- **Three-State Noninverting Outputs**
- **Propagation Delay . . . . 35ns Max.**
- **Gated Inputs:**
  - **Reduce Operating Power**
  - **Eliminate the Need for Pull-Up Resistors**
- **Single 5V Power Supply**
- **Low Power Operation . . . . ICCSB = 10µA**
- **Operating Temperature Ranges**
  - **C82C82 . . . . 0^oC to $+70^oC$**
  - **I82C82 . . . . -40^oC to $+85^oC$**
  - **M82C82 . . . . -55^oC to $+125^oC$**

Description

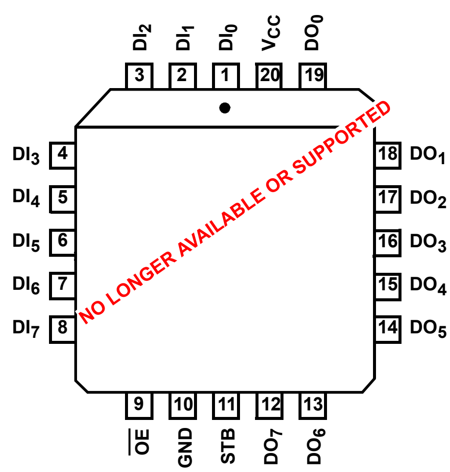
The Intersil 82C82 is a high performance CMOS Octal Latching Buffer manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C82 provides an eight-bit parallel latch/buffer in a 20 pin package. The active high strobe (STB) input allows transparent transfer of data and latches data on the negative transition of this signal. The active low output enable ($\overline{OE}$) permits simple interface to state-of-the-art microprocessor systems.

Pinouts

82C82 (PDIP, CERDIP)
TOP VIEW



82C82 (PLCC, CLCC)
TOP VIEW



TRUTH TABLE

STB	$\overline{OE}$	DI	DO
X	H	X	Hi-Z
H	L	L	L
H	L	H	H
↓	L	X	†

H = Logic One
L = Logic Zero
X = Don't Care
† = Latched to Value of Last Data
Hi-Z = High Impedance
↓ = Neg. Transition

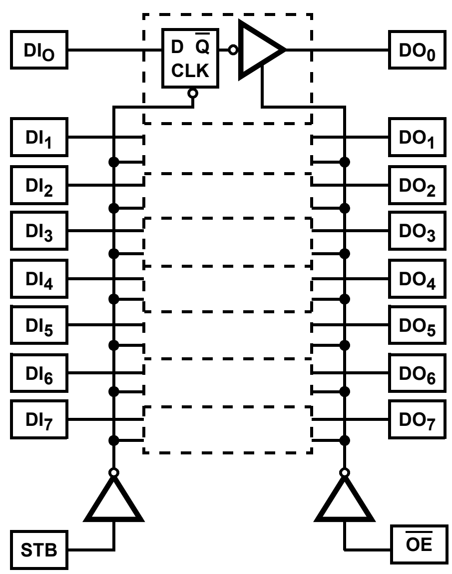
PIN NAMES

PIN	DESCRIPTION
DI_0-DI_7	Data Input Pins
DO_0-DO_7	Data Output Pins
STB	Active High Strobe
$\overline{OE}$	Active Low Output Enable

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
CP82C82 **(No longer available)**	$0^{o}C$ to $+70^{o}C$	20 Ld PDIP	E20.3
IP82C82 **(No longer available)**	$-40^{o}C$ to $+85^{o}C$		
CS82C82 **(No longer available)**	$0^{o}C$ to $+70^{o}C$	20 Ld PLCC	N20.35
IS82C82 **(No longer available)**	$-40^{o}C$ to $+85^{o}C$		
CD82C82 **(No longer available)**	$0^{o}C$ to $+70^{o}C$	20 Ld CERDIP	F20.3
ID82C82 **(No longer available)**	$-40^{o}C$ to $+85^{o}C$		
MD82C82/B **(No longer available)**	$-55^{o}C$ to $+125^{o}C$		
8406701RA		SMD #	
MR82C82/B **(No longer available)**	$-55^{o}C$ to $+125^{o}C$	20 Pad CLCC	J20.A
84067012A**(No longer available)**		SMD #	

Functional Diagram



Gated Inputs

During normal system operation of a latch, signals on the bus at the device inputs will become high impedance or make transitions unrelated to the operation of the latch. These unrelated input transitions switch the input circuitry and typically cause an increase in power dissipation in CMOS devices by creating a low resistance path between V_{CC} and GND when the signal is at or near the input switching threshold. Additionally, if the driving signal becomes high impedance ("float" condition), it could create an indeterminate logic state at the input and cause a disruption in device operation.

The Intersil 82C8X Series of bus drivers eliminates these conditions by turning off data inputs when data is latched (STB = logic zero for the 82C82/83H) and when the device is disabled ($\overline{OE}$ = logic one for 82C86H/87H). These gated inputs disconnect the input circuitry from the V_{CC} and ground power supply pins by turning off the upper P-channel and lower N-channel (see Figures 1, 2). No new current flow from V_{CC} to GND occurs during input transitions and invalid logic states from floating inputs are not transmitted. The next stage is held to a valid logic level internal to the device.

DC input voltage levels can also cause an increase in ICC if these input levels approach the minimum V_{IH} or maximum V_{IL} conditions. This is due to the operation of the input circuitry in its linear operating region (partially conducting state). The 82C8X series gated inputs mean that this condition will occur only during the time the device is in the trans parent mode (STB = logic one). ICC remains below the maximum ICC standby specification of l0mA during the time inputs are disabled, thereby, greatly reducing the average power dissipation of the 82C8X series devices

Typical 82C82 System Example

In a typical 80C86/88 system, the 82C82 is used to latch multiplexed addresses and the STB input is driven by ALE (Address Latch Enable) (see Figure 3). The high pulse width of ALE is approximately 100ns with a bus cycle time of 800ns (80C86/88 at 5MHz). The 82C82 inputs are active only 12.5% of the bus cycle time. Average power dissipation related to input transitioning is reduced by this factor also.

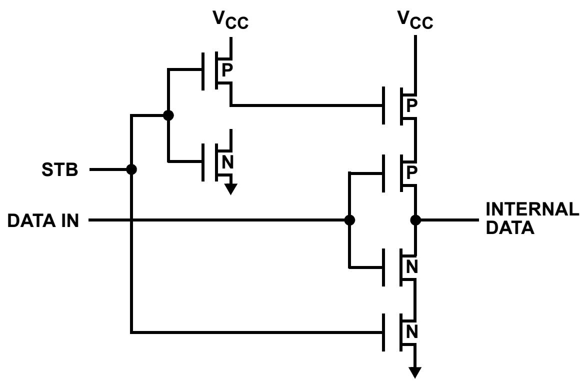


FIGURE 16. 82C82/83H

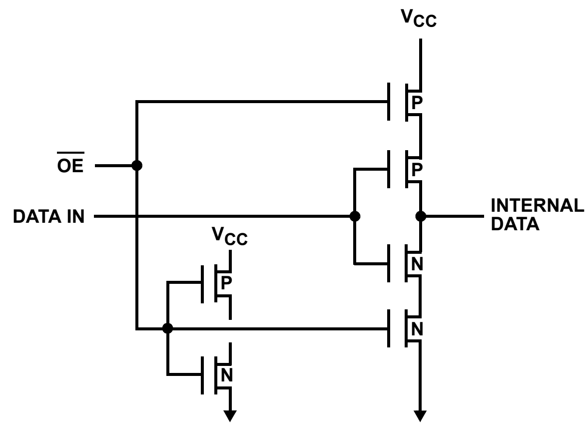


FIGURE 17. 82C86H/87H GATED INPUTS

Application Information

Decoupling Capacitors

The transient current required to charge and discharge the 300pF load capacitance specified in the 82C82 data sheet is determined by:

$$I = C_L (dv/dt) \quad \text{(EQ. 1)}$$

Assuming that all outputs change state at the same time and that dv/dt is constant;

$$I = C_L \quad \text{(EQ. 2)}$$

$$\frac{(V_{CC} \times 80\%)}{tR/tF} \quad \text{(EQ. 3)}$$

where tR = 20ns, V_{CC} = 5.0V, C_L = 300pF on each of eight outputs.

$$I = (8 \times 300 \times 10^{-12}) \times (5.0V \times 0.8)/(20 \times 10^{-9}) = 480mA \quad \text{(EQ. 4)}$$

This current spike may cause a large negative voltage spike on V_{CC}, which could cause improper operation of the device. To filter out this noise, it is recommended that a 0.1µF ceramic disc decoupling capacitor be placed between V_{CC} and GND at each device, with placement being as near

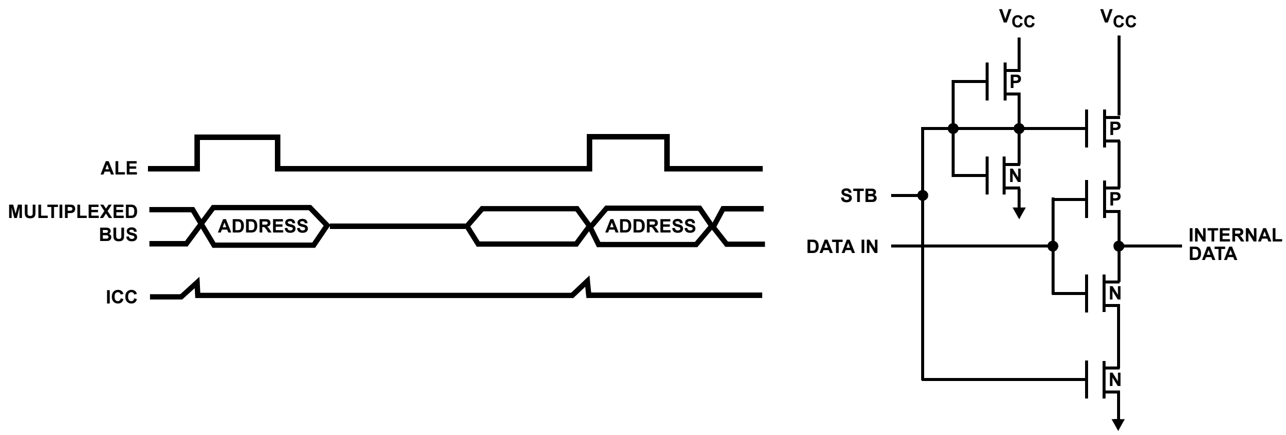


FIGURE 18. SYSTEM EFFECTS OF GATED INPUTS

Absolute Maximum Ratings

Supply Voltage . . . . +8.0V
Input, Output or I/O Voltage . . . . GND-0.5V to V_{CC} +0.5V
ESD Classification . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . +4.5V to +5.5V
Operating Temperature Range
C82C82 . . . . 0°C to +70°C
I82C82 . . . . -40°C to +85°C
M82C82 . . . . -55°C to +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
CERDIP	75°C/W	18°C/W
CLCC	85°C/W	22°C/W
PDIP	75	N/A
PLCC	75	N/A

Storage Temperature Range . . . . -65°C to +150°C
Maximum Junction Temperature
Ceramic Package . . . . +175°C
Plastic Package . . . . +150°C
Minimum Lead Temperature (Soldering 10s) . . . . +300°C
(PLCC Lead Tips Only)

Die Characteristics

Gate Count . . . . 65 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{CC} = 5.0V ±10%; T_A = 0°C to +70°C (C82C82); T_A = -40°C to +85°C (I82C82); T_A = -55°C to +125°C (M82C82)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0	-	V	C82C82, I82C82 (Note 1)
		2.2	-	V	M82C82 (Note 1)
V_{IL}	Logical Zero Input Voltage	-	0.8	V	

DC Electrical Specifications

V_{CC} = 5.0V ±10%; T_A = 0°C to +70°C (C82C82); T_A = -40°C to +85°C (I82C82); T_A = -55°C to +125°C (M82C82)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{OH}	Logical One Output Voltage	2.9	-	V	I_{OH} = -8mA, $\overline{OE}$ = GND
		V_{CC} -0.4V	-	V	I_{OH} = -100µA, $\overline{OE}$ = GND
V_{OL}	Logical Zero Output Voltage	-	0.4	V	I_{OL} = 8mA, $\overline{OE}$ = GND
II	Input Leakage Current	-1.0	1.0	µA	V_{IN} = GND or V_{CC}, DIP Pins 1-9, 11
IO	Output Leakage Current	-10.0	10.0	µA	V_O = GND or V_{CC}, $\overline{OE} \geq V_{CC}$ -0.5V DIP Pins 12-19
ICCSB	Standby Power Supply Current	-	10	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, Outputs Open
ICCOP	Operating Power Supply Current	-	1	mA/MHz	T_A = +25°C, V_{CC} = 5V, Typical (See Note 2)

NOTES:

1. V_{IH} is measured by applying a pulse of magnitude = V_{IH} min to one data input at a time and checking the corresponding device output for a valid logical "1" during valid input high time. Control pins (STB, $\overline{OE}$) are tested separately with all device data input pins at V_{CC} -0.4.
2. Typical ICCOP = 1mA/MHz of STB cycle time. (Example: 5MHz µP, ALE = 1.25MHz, ICCOP = 1.25mA).

Capacitance

T_A = +25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	13	pF	Freq = 1MHz, all measurements are referenced to device GND
C_{OUT}	Output Capacitance	20	pF	

AC Electrical Specifications

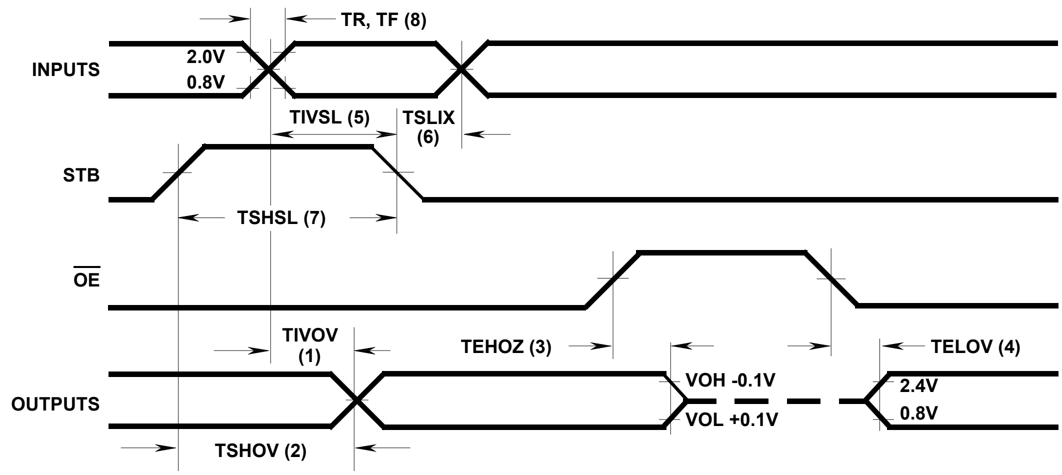
V_{CC} = 5.0V ±10%; C_L = 300pF (Note 1), Freq = 1MHz; T_A = 0°C to +70°C (C82C82); T_A = -40°C to +85°C (I82C82); T_A = -55°C to +125°C (M82C82)

SYMBOL		PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1)	TIVOV	Propagation Delay Input to Output	-	35	ns	Notes 2, 3
(2)	TSHOV	Propagation Delay STB to Output	-	55	ns	Notes 2, 3
(3)	TEHOZ	Output Disable Time	-	35	ns	Notes 2, 3
(4)	TELOV	Output Enable Time	-	50	ns	Notes 2, 3
(5)	TIVSL	Input to STB Setup Time	0	-	ns	Notes 2, 3
(6)	TSLIX	Input to STB Hold Time	25	-	ns	Notes 2, 3
(7)	TSHSL	STB High Time	25	-	ns	Notes 2, 3
(8)	TR, TF	Input Rise/Fall Times	-	20	ns	Notes 2, 3

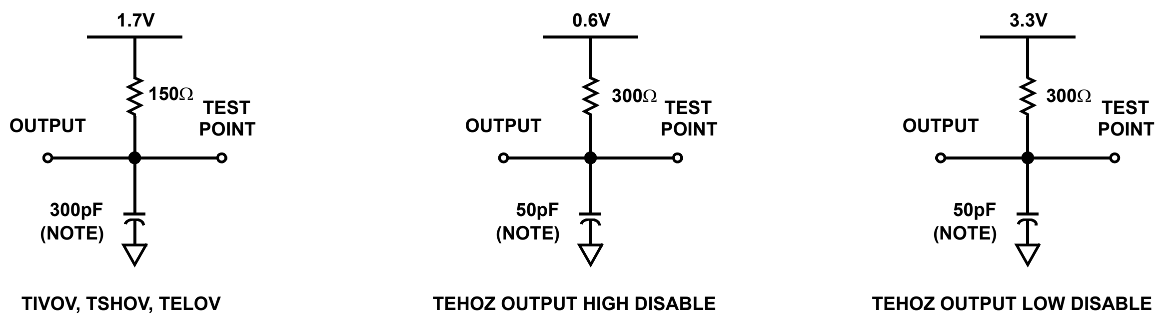
NOTES:

1. Output load capacitance is rated at 300pF for ceramic and plastic packages.
2. All AC parameters tested as per test circuits and definitions below. Input rise and fall times are driven at 1ns/V.
3. Input test signals must switch between V_{IL} - 0.4V and V_{IH} +0.4V.

Timing Waveforms



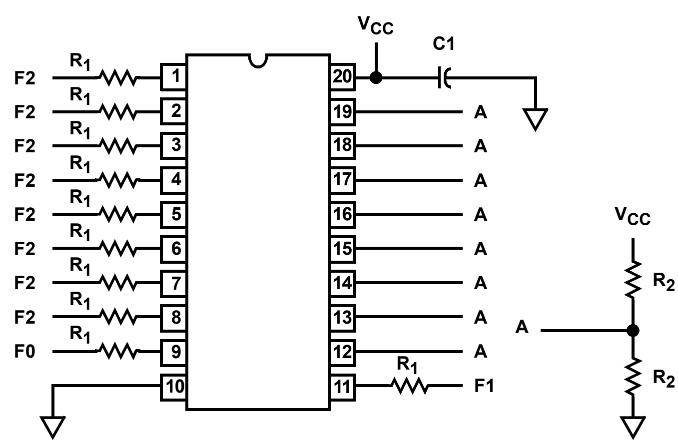
Test Load Circuits



NOTE: Includes stray and jig capacitance.

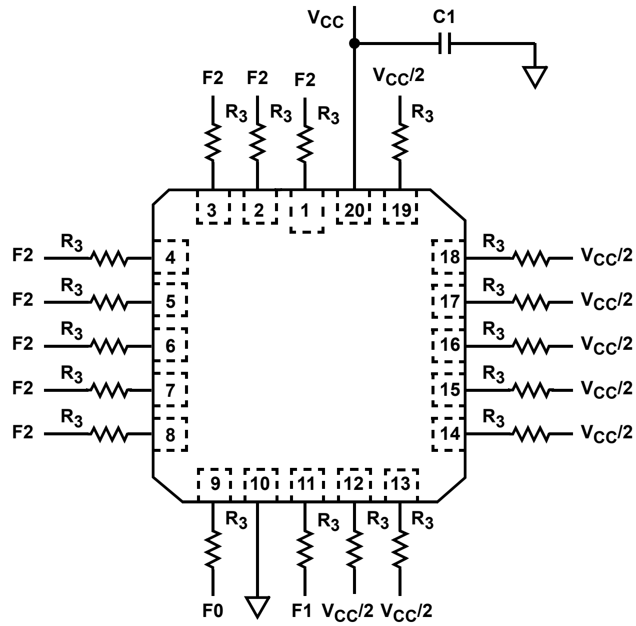
Burn-In Circuits

MD82C82 CERDIP



Burn-In Circuits

MR82C82 CLCC



NOTES:

1. V_{CC} = 5.5 ± 0.5V, GND = 0V.
2. V_{IH} = 4.5V ±10%.
3. V_{IL} = -0.2V to 0.4V.
4. R_1 = 47kΩ ±5%.
5. R_2 = 2.0kΩ ±5%.
6. R_3 = 4.2kΩ ±5%.
7. R_4 = 470kΩ ±5%.
8. C_1 = 0.01μF minimum.
9. F_0 = 100kHz ±10%.
10. $F_1 = F_0/2$, $F_2 = F_1/2$.

Die Characteristics

DIE DIMENSIONS:
118.1 x 92.1 x 19 ±1mils

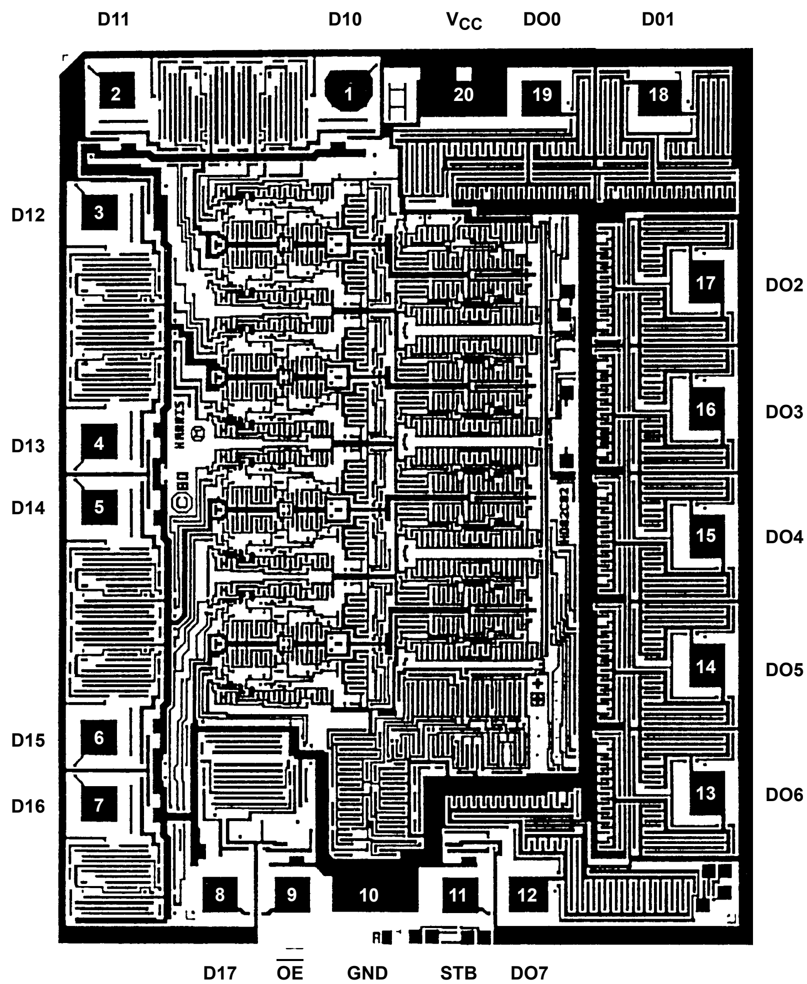
METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ±1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
2.00×10^5 A/cm^2

Metallization Mask Layout

82C82



Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
August 25, 2015	FN2975.2	- Ordering Information Table on page 2. - Added Revision History. - Added About Intersil Verbiage.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support